Amendments to the Specification:

Please replace the paragraph beginning at page 11, line 5, with the following amended paragraph:

Figure 2 represents a functional block diagram of the computer network shown in Figure 1. The computer 100 ~~generally includes~~ comprises a central processor unit (CPU) 202, a main memory array 204, and a bridge logic device 206 coupling the CPU 202 to the main memory 204. The bridge logic device is sometimes referred to as a "North bridge" for no other reason than it often is depicted at the upper end of a computer system drawing. The North bridge 206 couples the CPU 202 and memory 204 to various peripheral devices in the system through a primary expansion bus (Host Bus) such as a Peripheral Component Interconnect (PCI) bus or some other suitable architecture.

Please replace the paragraph beginning at page 11, line 17, with the following amended paragraph:

Various peripheral devices that implement the host bus protocol may reside on the host bus. For example, a modem 216, and network interface card (NIC) 218 are shown coupled to the host bus in Figure 2. The modem 216 ~~generally~~ allows the computer to communicate with other computers or facsimile machines over a telephone line, an Integrated Services Digital Network (ISDN), or a cable television connection, and the NIC 218 permits communication between computers over a local area network (LAN) (e.g., an Ethernet network card or a Cardbus card). These components may be integrated into the motherboard or they may be plugged into expansion slots that are connected to the host bus.

Please replace the paragraph beginning at page 12, line 3, with the following amended paragraph:

Figure 2 also depicts a host channel adapter (HCA) 220 connected to the host bus and target channel adapters (TCA) 230, 240 connected to the external network devices 110, 120. These channel adapters ~~generally~~ provide address and translation capability for the switched topology architecture in the preferred

embodiment. The channel adapters 220, 230, 240 preferably have dedicated IPv6 (Internet Protocol Version 6) addresses that can be recognized by the network switch 130. As data is transmitted to the network, the source file is divided into packets of an efficient size for routing. Each of these packets is separately numbered and includes the address of the destination. When the packets have all arrived, they are reassembled into the original file. The network switch 130 in this preferred embodiment can detect the destination address, and route the data to the proper location.

Please replace the paragraph beginning at page 12, line 13, with the following amended paragraph:

Figure 2 also shows the physical links 140 between the network devices as ~~simple~~ two lane links. In the embodiment shown in Figure 2, data would flow through one lane in one direction while data would flow through the parallel lane the other direction. As discussed above, alternative embodiments comprising any even number of lanes are also permissible, with 2, 8, and 24 lanes per link being the preferred number.

Please replace the paragraph beginning at page 12, line 18, with the following amended paragraph:

Figure 3 shows an alternative embodiment of the computer network in which the computer 100 is replaced by a server 300 with a ~~simple~~ memory-processor architecture. Such a server may be part of a cluster of servers, a group of several servers that share work and may be able to back each other up if one server fails. In this particular embodiment, the server 300 is coupled to the switched-fabric network in much the same way the computer 100 of Figure 1 is connected. The physical link 140 is connected to the server via a host channel adapter (HCA) 220. However, in this embodiment, the HCA 220 is connected directly to a North Bridge 206. Alternatively, the HCA 220 may be connected directly to a memory controller. In either event, a shared peripheral bus, such as a PCI bus, is not necessary in this embodiment. A peripheral bus may still be

used in the server 300, but is preferably not used to couple the north bridge 206 to the HCA 220.

Please replace the paragraph beginning at page 18, line 20, with the following amended paragraph:

As discussed above, the Infiniband links will implement 1, 4, or 12 lanes in each direction. The Infiniband specification further imposes requirements to support mixed bus widths. An automatic link configuration routine will determine the width supported by the link and the two ports. Thus, when mixed bus widths are connected serially, the ports will only transmit data through the smaller quantity of lanes. For example, when a 12 lane link is coupled to a to a 4 lane link, only 4 of the 12 lanes in the former link will be used. Correction of lane reversal errors must consider all combinations of bus widths to guarantee that the signals traveling through the physical media are in the correct order. Figure 9 shows the possible combinations for Infiniband links. The combinations in Figure 9 are ~~generally~~ grouped into three columns with the left most column showing a 1 lane transmitter 900 coupled to 1, 4, and 12 lane receivers. The center column shows a 4 lane transmitter 910 coupled to 1, 4, and 12 lane receivers and the right most column shows a 12 lane transmitter 920 coupled to 1, 4, and 12 lane receivers. Lane reversal is not an issue in a 1 to 1 connection, but it is included in Figure 9 in the interest of thoroughness.

Please replace the paragraph beginning at page 20, line 1, with the following amended paragraph:

Lane reversal errors including the example above may be corrected via a bank of 2 to 1 multiplexers configured to reorder the individual lanes in a physical link. Figure 10 shows the multiplexer logic necessary in the receiver and transmitter of a 4 lane port. Figure 11 shows the multiplexer logic necessary in the receiver and transmitter of a 12 lane port. Multiplexers are ~~conventionally~~ used to combine several signals for transmission on some shared medium. In this preferred embodiment, the multiplexers are logic devices configured to

transmit a selected one of the two input signals as necessary to change the order of the incoming signals.